REMARKS

This is a full and timely response the outstanding non-final Office Action mailed on May 16, 2003 (Paper No. 21). Claims 1, 2, 4-10, 17, 18, 20, and 21 are pending in the Application. More specifically, claims 1, 2, 6, 17, 18, 20, and 21 are directly amended. Reconsideration and allowance of the Application and presently pending claims 1, 2, 4-10, 17, 18, 20, and 21 are respectfully requested.

I. Response to Claim Objections

Claim 20 stands rejected under 37 C.F.R. 1.75(c) as being in improper dependent form for failing to further limit the subject matter of a previous claim. Applicants have amended claim 20 and request that the rejection be withdrawn.

II. Response to Claim Rejection Under 35 U.S.C. §103

In the Office Action, claims 1-2, 4-5, 17-18, and 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) (hereinafter AAPA) in view of U.S. Patent No. 6,043,704, to Yoshitake (hereinafter *Yoshitake*). Claims 6-10 and 21 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over AAPA in view of *Yoshitake* and further in view of U.S. Patent No. 6,140,686, to Mizuno (hereinafter *Mizuno*).

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a single reference, the reference must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. *See, e.g., In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that the proposed combination of AAPA in view of *Yoshitake* fails to disclose, teach or suggest each and every element of claims 1-2, 4-5, 17-18, and 20 for at least the reasons that follow. Further, Applicants respectfully submit that the proposed combination of AAPA in view of *Yoshitake* and further in view of *Mizuno* fails to disclose, teach or suggest each and every element of claims 6-10 and 21 for at least the reasons that follow.

A. Claim 1

Claim 1, as amended, recites:

> An integrated circuit comprising:
> a first port for outputting a signal;
> a second port for receiving said signal;
> a common area comprising an alignment link for electrically connecting said first port with said second port;

> ***said first port is directly and electrically <u>wired</u> <u>traced</u> to said alignment link*** from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;
>
> said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area; and
>
> said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; said alignment link is arranged within said common area.

(Emphasis Added)

Applicants would like to point out that in the final Office Action mailed May 16, 2003 (Paper No. 21), <u>the Office Action admitted that AAPA (Figs. 1 and 2) fails to disclose that the first port is directly and electrically connected to the alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with the first port and the common area</u>. In this regard, the Office Action uses *Yoshitake* to allegedly disclose an input driver 11 for outputting a signal; a buffer 12 for receiving an output of the driver 11 (Fig. 1, column 7, lines 10-20), wherein the driver 11 is directly and electrically connected to the alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with the first port and the common area to provide a clock distribution circuit and can realize reduction in skew (Office Action at page 3, lines 13-18).

Applicants respectfully submit that *Yoshitake* fails to teach, disclose or suggest at least the above-emphasized element as recited in amended claim 1. *Yoshitake* apparently appears to disclose at most a schematic view of a clock distribution circuitry for a semi-conductor integrated circuit, which quite different from "said first port is directly and electrically <u>wired traced</u> to said alignment link" (emphasis added), as recited in amended claim 1. Applicants respectfully submit that *Yoshitake* fails to teach, disclose or suggest a physical layout and/or placement for aligning ports and providing for a signal buffering within a common area of integrated circuit real estate.

Consequently, as admitted in the Office Action (Paper No. 21), AAPA (Figs. 1 and 2) fails to disclose that the first port is directly and electrically connected to the alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with the first port and the common area. Thus, Applicants respectfully

submit that AAPA fails to disclose, teach or suggest "said first port is directly and electrically wired traced to said alignment link" (emphasis added), as recited in amended claim 1. Further, as discussed above, Applicants respectfully submit that *Yoshitake* fails to disclose, teach or suggest "said first port is directly and electrically wired traced to said alignment link" (emphasis added), as recited in amended claim 1. Accordingly, the proposed combination of AAPA in view *Yoshitake* fails to disclose, teach or suggest "said first port is directly and electrically wired traced to said alignment link," as recited in amended claim 1. For this reason alone, Applicants respectfully request that amended claim 1 be allowed and the rejection be withdrawn.

B. Claims 2 and 4-5

Because independent claim 1 is allowable over the cited art of record, dependent claims 2 and 4-5 are allowable as a matter of law for at least the reason that dependent claims 2 and 4-5 contain all features and elements of their respective independent base claim. *See e.g., In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, Applicants respectfully submit that the rejection to dependent claims 2 and 4-5 be withdrawn for this reason alone.

C. Claim 6

Independent claim 6, as amended, includes "said first port is directly and electrically wired traced to said link alignment" (emphasis added).

For at least the reasons set forth hereinabove in the arguments for the allowability of claim 1, Applicants respectfully submit that the proposed combination of AAPA in view of *Yoshitake* fails to disclose, teach or suggest at least the feature of claim 6 cited above.

Further, the Office Action (Paper No. 21) appears to cite *Mizuno* for disclosing an integrated circuit comprising multi-levels wherein the multi-levels have a semiconductor level and a wiring level. However, *Mizuno* fails to remedy *Yoshitake* and AAPA, which fail to disclose, teach or suggest at least the feature of claim 6 cited above. Accordingly, the proposed combination of the AAPA in view of *Yoshitake*, and further in view *Mizuno* fails to disclose, teach or suggest at least the feature of "said first port is directly and electrically wired traced to said link alignment" (emphasis added), as recited in amended claim 6. For this reason alone, Applicants respectfully request that amended claim 6 be allowed and the rejection be withdrawn.

D. Claims 7-10

Because independent claim 6 is allowable over the cited art of record, dependent claims 7-10 are allowable as a matter of law for at least the reason that dependent claims 7-10

contain all features and elements of their respective independent base claim. *In re Fine, supra*. Accordingly, Applicants respectfully submit that the rejection to dependent claims 7-10 be withdrawn for this reason alone.

E. Claim 17

Independent claim 17, as amended, includes "said first port is directly and electrically wired traced to said alignment means" (emphasis added).

For at least the reasons set forth hereinabove in the arguments for the allowability of claim 1, Applicants respectfully submit that the proposed combination of AAPA in view of *Yoshitake* fails to disclose, teach or suggest at least the feature of claim 17 cited above. For this reason alone, Applicants respectfully request that amended claim 17 be allowed and the rejection be withdrawn.

F. Claims 18 and 20

Because independent claim 17 is allowable over the cited art of record, dependent claims 18 and 20 are allowable as a matter of law for at least the reason that dependent claims 18 and 20 contain all features and elements of their respective independent base claim. *In re Fine, supra*. Accordingly, Applicants respectfully submit that the rejection to dependent claims 18 and 20 be withdrawn for this reason alone.

G. Claim 21

Independent claim 21, as amended, includes "said set of output ports of said first area is directly and electrically connected to said first set of wiring traces of said buffering blocks without the use of a first linking area that includes bridge traces for linking mis-aligned ports with said first port and said common area" (emphasis added).

For at least the reasons set forth hereinabove in the arguments for the allowability of claim 1, Applicants respectfully submit that the proposed combination of AAPA in view of *Yoshitake* fails to disclose, teach or suggest at least the feature of claim 21 cited above.

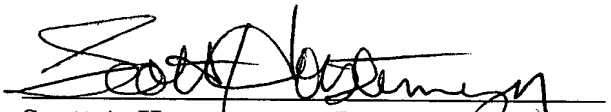
Further, the Office Action (Paper No. 21) appears to cite *Mizuno* for disclosing an integrated circuit comprising multi-levels wherein the multi-levels have a semiconductor level and a wiring level. However, *Mizuno* fails to remedy *Yoshitake* and AAPA, which fail to disclose, teach or suggest at least the feature of claim 21 cited above. Accordingly, the proposed combination of the AAPA in view of *Yoshitake*, and further in view *Mizuno* fails to disclose, teach or suggest at least the feature of "said set of output ports of said first area is directly and electrically connected to said first set of wiring traces of said buffering blocks without the use of a first linking area that includes bridge traces for linking mis-aligned ports

with said first port and said common area" (emphasis added), as recited in claim 21. For this reason alone, Applicants respectfully request that claim 21 be allowed and the rejection be withdrawn.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1, 2, 4-10, 17, 18, 20 and 21 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned at (770) 933-9500.

Respectfully submitted,



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